


INFORMATION DISCLOSURE CITATION IN AN APPLICATION 				ATTY. DOCKET NO. 61282-011		SERIAL NO. 09/801,200	
				APPLICANT Kenji SHIMAZAKI, et al.			
				FILING DATE March 08, 2001		GROUP 2857	
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
8	5,903,477	5/11/1999	Otsu et al.			RECEIVED OCT 11 2002 TECHNOLOGY CENTER 2800	
FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
8	2001-22813	1/26/2001	Japan (w/ English Abstract)				
	DE19816192A1	4/8/1999	Germany				
	DE19826236A1	6/2/1999	Germany				
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER <i>Shamha Patel</i>				DATE CONSIDERED 6/17/06			

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

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 ATTY. DOCKET NO.
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Kenji SHIMAZAKI, et al.

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GROUP

 J1044 U.S. PTO
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U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
W	5,412,589	5/2/95	Williams et al.			
S	5,675,832	10/7/97	Ikami et al.			
N	5,699,263	12/16/97	Nakao			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

W	"di/dt Noise in CMOS Integrated Circuits", by Patrik Larsson, Analog Integrated Circuits and Signal Processing, Vol. 14 (1997), pp. 113-129.
S	"EMI-Noise Analysis Under ASIC Design Environment", by Sachio Hayashi et al., International Symposium on Physical Design (1999), pp. 16-21.
S	"Power Supply Noise Analysis Methodology for Deep-Submicron VLSI Chip Design", by Howard Chen et al., DAC97, pp. 1-6.
S	"Design Methodologies for Noise in Digital Integrated Circuits", by Kenneth Shepard, DAC98 (June 1998).

EXAMINER



DATE CONSIDERED

6/14/06

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